A computational approach for improving the manufacturing yield of monolithic 3D integrated circuits

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Unmet Need

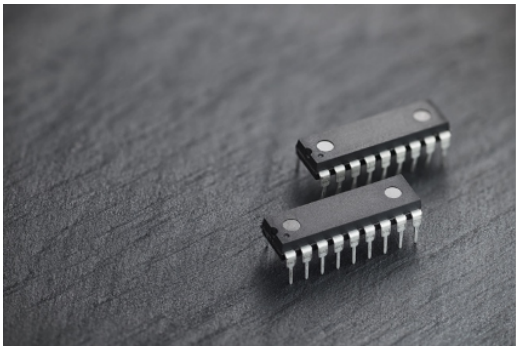
3D integrated circuits (ICs) have emerged as a promising solution for improving performance, increasing functionality, and reducing power consumption in semiconductors and microelectronics. Monolithic 3D integrated circuits (M3D ICs) provides an alternative to scaling by drastically reducing the vertical distance between circuit layers, making it possible to truly design in 3D. However, the sequential vertical assembly of M3D tiers and immature fabrication process are prone to manufacturing defects and inter-tier process variations. Existing testing strategies do not address the problem of fault localization in M3D ICs. Thus, advances in testing tools for low-overhead fault detection and localization are needed to improve yield and help bring M3D chips toward mass manufacturing.

Technology

Researchers at Duke have developed a new computational approach for localizing faults in monolithic 3D integrated circuits. This technology is intended to be applied after production testing of an M3D chip to provide feedback regarding pitfalls in manufacturing and design rules. A ranking algorithm was used to localize faults to a particular tier of the 3D chip. This computationally efficient method can select a small set of outgoing inter-layer vias (ILVs) for observation-point insertion (OPI) in M3D ICs. To increase the overall testability and fault localization, NodeRank algorithm was integrated with commercial design-for-testability (DfT) tools. The inventors have demonstrated the scalability of NodeRank-based OPI heuristics and their synergy with a commercial DfT tool by inserting OPs in three-tier M3D designs.

Advantages

- Provides feedback regarding pitfalls in manufacturing that can improve yield ramp-up in the manufacturing of M3D ICs for semiconductors and microelectronics
- Does not rely on extensive fault simulations
- Several orders-of-magnitude faster than standard ATPG fault simulation-based OPI



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Links

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- Significantly improve observation point analysis without adversely impacting power, performance, and area
- Integration with DfT tools offers more effective fault localization and testability

Publications

- Test and Design-for-Testability Solutions for Monolithic 3D Integrated Circuits (GLSVLSI, 2019)
- Built-in Self-Test for Inter-Layer Vias in Monolithic 3D ICs (IEEE, 2019)
- A design-for-test solution based on dedicated test layers and test scheduling for monolithic 3D integrated circuits (IEEE, 2019)
- An inter-layer interconnect BIST and diagnosis solution for monolithic 3D ICs (IEEE, 2018)