Recycled error bits: architectural support for energy-efficient and numerically accurate software

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Value proposition

Computer perform extensive amount of calculations which is carried out by the floating point hardware. The finite precision of floating point hardware provides a potential for small inaccuracies to result in larger, glaring inaccuracies over the course of a long sequence of computations. Many traditional approaches are used to handle this well-know problem. This includes Maximum Hardware Precision, Mixed Hardware Precision, Emulating Greater Precision with Software, etc. All of these traditional techniques have significant energy and performance overheads drawbacks.

Technology

This work may have found a solution to this problem. It provides energy-efficient architectural support for floating point accuracy. For each floating point addition performed, that operation’s rounding error is “recycled”. This error is architecturally visible such that it can be used, whenever desired, by software. A compiler pass is designed to allow software to automatically use this feature. Experimental results on physical hardware show that software that exploits architecturally recycled error bits can (a) achieve accuracy comparable to a 64-bit FPU with performance and energy that are comparable to a 32-bit FPU, and (b) achieve accuracy comparable to an all-software scheme for 128-bit accuracy with far better performance and energy usage.

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