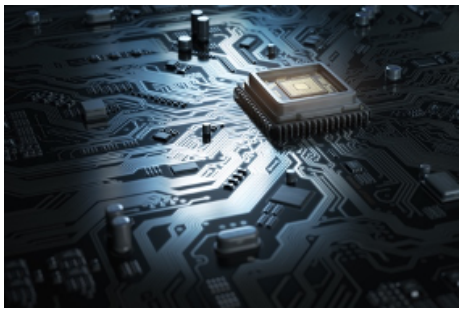
A fault detection method to improve the high-volume manufacturing of energy efficient carbon nanotube field-effect transistors

Unmet Need

Carbon nanotube field-effect transistors (CNFETs) have emerged as one of the most promising tools to improve the energy efficiency of next-generation integrated circuits (ICs), which are used in virtually all electronic equipment. However, the immature CNFET fabrication process often leads to variations and manufacturing defects which can hinder their high-volume manufacturing. Conventional test-generation methods are limited in their utility to detect variations-induced faults in CNFETs. Thus, there is a need for improved delay fault testing in carbon nanotube FET-based logic circuits.

Technology

Researchers at Duke have developed a method to test for manufacturing faults in ICs based on CNFETs. This technology is intended to improve the manufacturing feasibility of CNFETs and enable their application as a more energy efficient integrated circuit for computers, smart phones, and other electronics. Specifically, this technology takes CNFET-specific process variations into account and identifies multiple testable long paths through each node in a netlist, as part of an end-to-end IC design process. It ensures the detection of delay faults through the longest fault, even under random CNFET process variations. The variation-aware delay fault method was integrated with the existing commercial EDA tool to create an efficient and nondestructive end-to-end delay fault testing flow. Simulation results for multiple benchmarks showed significantly improved coverage and test pattern grading.



Duke File (IDF) Number

IDF #:T-007167

Meet the Inventors

Banerjee, Sanmitra
Chakrabarty, Krishnendu

Department

Electrical & Computer Engineering (ECE)

Publication(s)

External Link(s)

- From the lab of Dr. Krishnendu Chakrabarty

Advantages

- Enables high-volume manufacturing of CNFETs for application in electronic equipment
- Takes CNFET-specific process variations into account when identifying faults
- Can be used to improve existing commercial tools due to ease of integration with conventional IC design flow
- Shows significant improvement in the statistical delay quality level compared to state-of-the-art technique and a commercial EDA tool